Amendments to the Specification:

Please replace paragraph **[0022]** with the following rewritten paragraph:

Exposed portions of the upper and lower surfaces of resin layer 111, the conductive surface 114, and the circuit patterns 113 may be coated with a protective layer 115, except over bond fingers 116 and ball lands ~~115~~ 117. The protective layer 115 serves to protect the substrate 110 from the external environment. The protective layer 115 may be an epoxy-based resin material.

Please replace paragraph **[0043]** with the following rewritten paragraph:

Electrically conductive vias ~~313~~ 318 extending vertically through the resin layer 311 electrically couple the circuit patterns 314 of the upper surface of resin layer 311 to the circuit patterns 313 on the lower surface of resin layer 311. The circuit patterns 313 include ball lands 317 to which the solder balls 370 are fused. Here, both the lower circuit patterns 313 and the upper circuit patterns 314 are made from Cu, Au, Al or their equivalent. A protective layer 315 for protecting the substrate 310 from an external environment is provided on both the upper and lower surfaces of resin layer 311, but does not cover the bond fingers 316 and ball lands 317 of circuit patterns 313 and 314.

Please replace paragraph **[0053]** with the following rewritten paragraph:

Note that, in semiconductor package 400, the circuit patterns 414 on the upper surface of resin layer ~~414~~ 411 include ball lands 417 as well as bond

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888

fingers 416. Accordingly, to provide a stack of semiconductor packages, the solder balls 371, 372 of an upper semiconductor package 300, may be fused to the upper ball lands 417 of the lower semiconductor package 400 in order to electrically couple the semiconductor packages 300 and 400. With such a configuration, the semiconductor dies 320, 420 of the stacked packages may electrically communicate with each other, and/or may each be electrically accessed through the solder balls 470, circuit patterns 413 and 414, and vias 418 of the lower semiconductor package 400.

Please replace paragraph **[0055]** with the following rewritten paragraph:

In one application, semiconductor package 400 may be used to house a logic device semiconductor die 420, which would tend to have a relatively large number of bond pads 421. Such a package, with a relatively large number of solder balls 470, will tend to have a smaller area through hole ~~414~~ 412 relative to the area of through hole 312 of semiconductor package 300, and hence should be less susceptible to post-encapsulation warpage. Semiconductor package 300 may be used to house a memory device semiconductor die 320, which would tend to have a relatively fewer number of bond pads 321 and solder balls 371, 372, and a relatively larger area through hole 312. The larger area through hole 312 compared to the area of through hole 412 makes post-encapsulation warpage of semiconductor package 300 more likely than warpage of semiconductor package 400.

GUNNISON, McKAY & HODGSON, L.L.P.
Garden West Office Plaza
1900 Garden Road, Suite 220
Monterey, CA 93940
(831) 655-0880
Fax (831) 655-0888